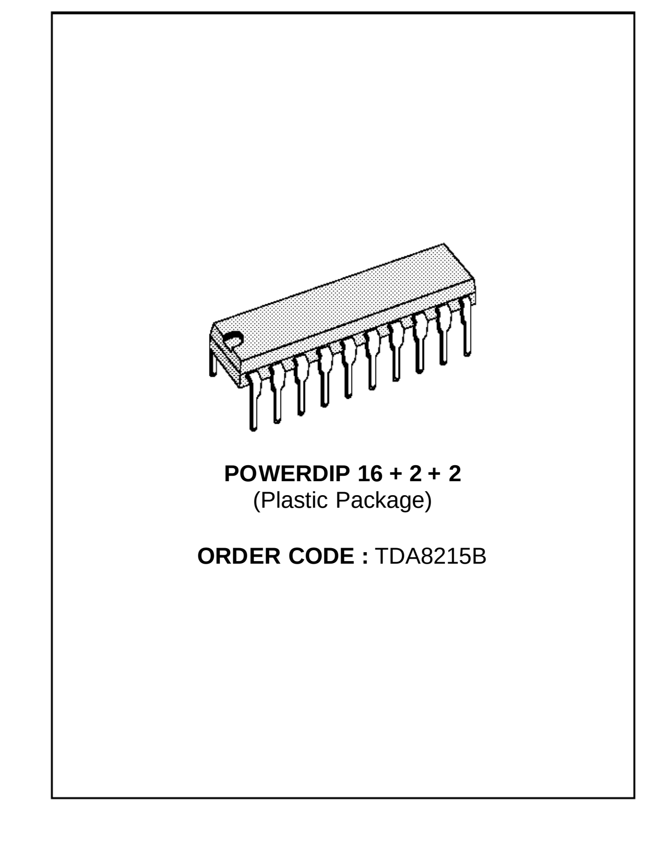


TDA8215B

HORIZONTAL AND VERTICAL DEFLECTION CIRCUIT

- DIRECT LINE DARLINGTON DRIVE
- DIRECT FRAME-YOKE DRIVE (± 1A)
- COMPOSITE VIDEO SIGNAL INPUT CAPABILITY
- FRAME OUTPUT PROTECTION AGAINST SHORT CIRCUITS
- PLL
- VIDEO IDENTIFICATION CIRCUIT
- SUPER SANDCASTLE OUTPUT
- VERY FEW EXTERNAL COMPONENTS
- VERY LOW COST POWER PACKAGE



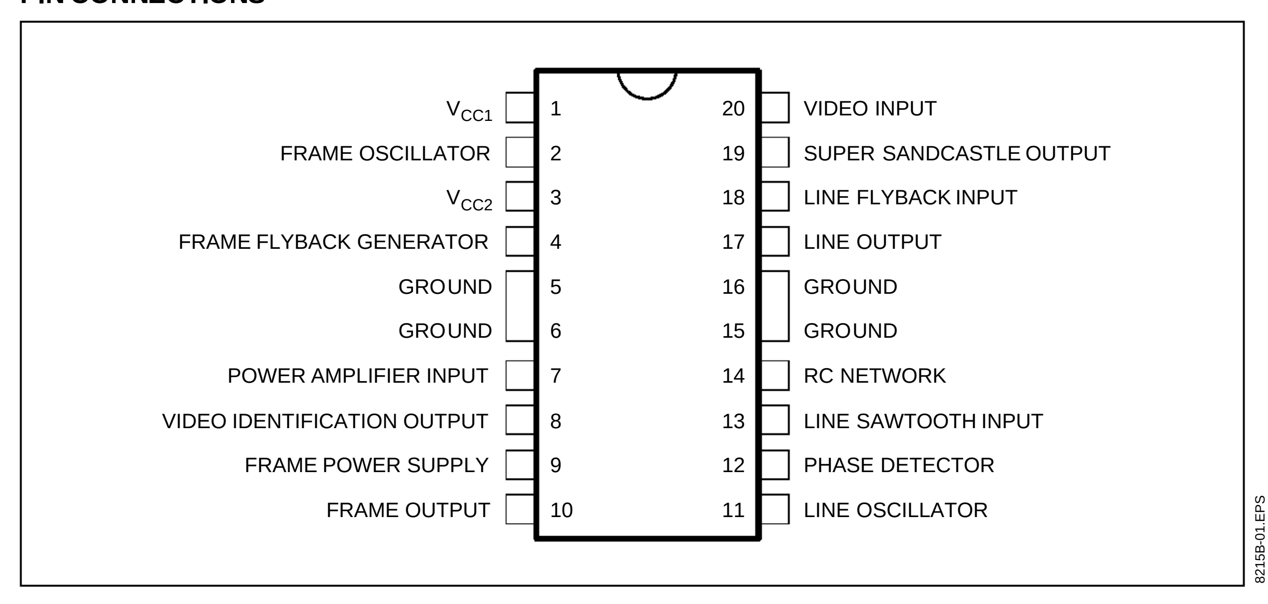
POWERDIP 16 + 2 + 2
(Plastic Package)

ORDER CODE : TDA8215B

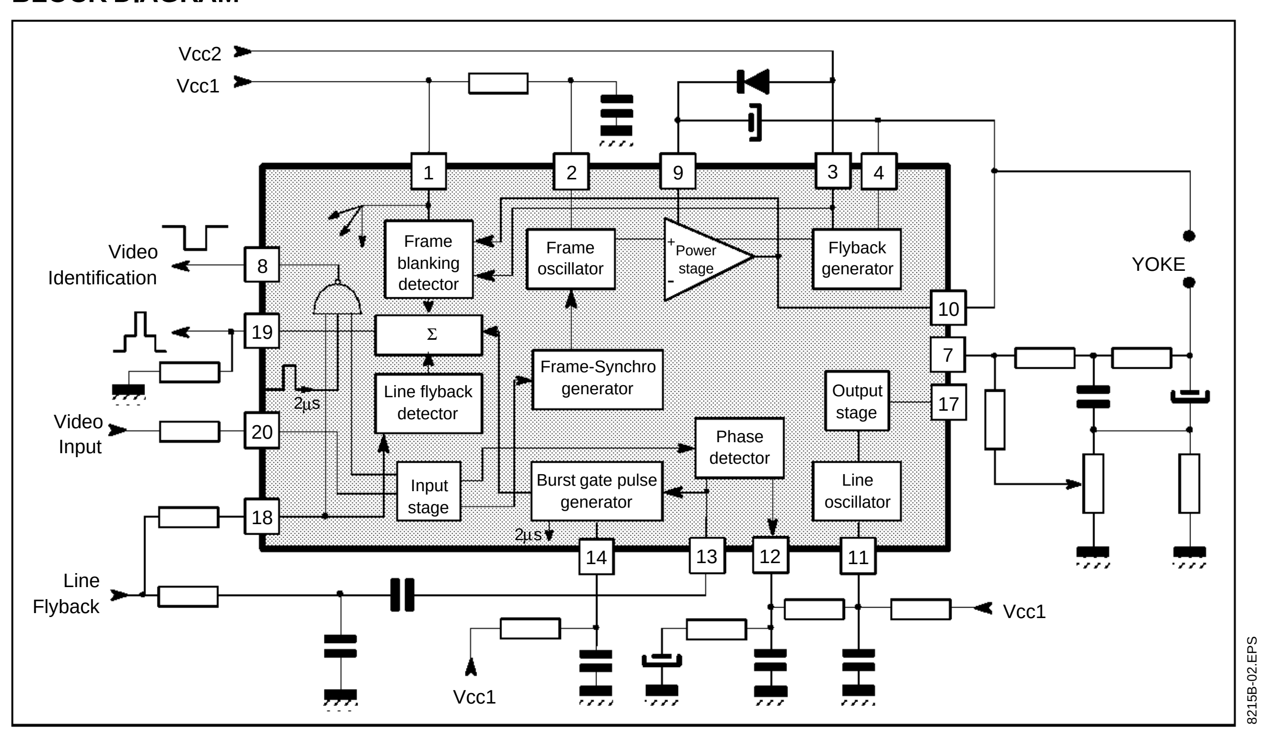
DESCRIPTION

The TDA8215B is an horizontal and vertical deflection circuit with super sandcastle generator and video identification output. Used with TDA8213 (Video & Sound IF system) and TDA8217 (Pal decoder and video processor), this IC permits a complete low-cost solution for PAL applications. The TDA8215B has been specially designed for direct drive of line DARLINGTON transistors.

PIN CONNECTIONS



BLOCK DIAGRAM



8215B-02.EPS

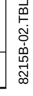
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}1$	Supply Voltage	30	V
$V_{CC}2$	Flyback Generator Supply Voltage	35	V
V9	Frame Power Supply Voltage	60	V
$I10_{NR}$	Frame Output Current (non repetitive)	± 1.5	A
I10	Frame Output Current (continuous)	± 1	A
V17	Line Output Voltage (external)	60	V
I_P17	Line Output Peak Current	0.8	A
I_C17	Line Output Continuous Current	0.4	A
T_{STG}	Storage Temperature	-40 to + 150	°C
T_J	Max Operating Junction Temperature	+ 150	°C
T_{AMB}	Operating Ambient Temperature	0 to 70	°C

8215B-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{TH(j-c)}$	Max Junction-case Thermal Resistance	10	°C/W
$R_{TH(j-a)}$	Typical Junction-ambient Thermal Resistance *(Soldered on a 35µm thick 45cm² PC Board copper area)*	40	°C/W
T_J	Max Recommended Junction Temperature	120	°C



ELECTRICAL CHARACTERISTICS

V_{CC1} = 10V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SUPPLY (Pin 1)					
I_{CC1}	Supply Current		15		mA
V_{CC1}	Supply Voltage	9	10	10.5	V
VIDEO INPUT (Pin 20)					
V20	Reference Voltage (I_{20} = -1µA)	1.4	1.75	2	V
MWF	Minimum Width of Frame Pulse (When synchronized with TTL signal)	50			µs
LINE OSCILLATOR (Pin 11)					
LT11	Low Threshold Voltage	2.8	3.2	3.6	V
HT11	High Threshold Voltage	5.4	6.6	7.8	V
BI11	Bias Current		100		nA
DR11	Discharge Impedance	1.0	1.4	1.8	kΩ
FLP1	Free Running Line Period (R = 34.9kΩ Tied to V_{CC1}, C = 2.2nF Tied to Ground)	62	64	66	µs
FLP2	Free Running Line Period (R = 13.7KΩ, C = 2.2nF)		27		µs
OT11	Oscillator Threshold for Line Output Pulse Triggering		4.6		V
$\frac{\Delta F}{\Delta \theta}$	Horizontal Frequency Drift with Temperature (see application)		2		Hz/°C
LINE OUTPUT (Pin 17)					
LV17	Saturation Voltage (I_{17} = 800mA during 2µs)		2.2		V
OPW	Output Pulse width (line period = 64µs , negative pulse)	19	21	23	µs
LINE SAWTOOTH INPUT (Pin 13)					
V13	Bias Voltage	1.8	2.4	3.2	V
Z13	Input Impedance	4.5	5.8	8	kΩ
PHASE DETECTOR (Pin 12)					
I12	Output Current During Synchro Pulse	250	350	500	µA
RI12	Current Ratio (positive/negative)	0.95	1	1.05	
LI12	Leakage Current	-2		+2	µA
CV12	Control Voltage Range	2.60		7.10	V
VIDEO IDENTIFICATION (Pin 8)					
	Low Level Output when the line synchro tip is centered in the line retrace				
V_{H8}	without Video Signal (I_8 = -500µA)	4.5	6.3	0.9	V
V_{L8}	with Video Signal (I_8 = 50µA)		0.6	0.9	V
FRAME OSCILLATOR (Pin 2)					
LT2	Low Threshold Voltage	1.6	2.0	2.3	V
HT2	High Threshold Voltage	2.6	3.1	3.6	V
DIF2	LT2 - HT2		1.0		V
BI2	Bias Current		30		nA
DR2	Discharge Impedance	300	470	700	Ω
FFP1	Free Running Frame Period (R = 845kΩ Tied to V_{CC1}, C = 180nF Tied to Ground)	20.5	23	25	ms
MFP	Minimum Frame Period (I_{20} = -100µA) with the Same RC		12.8		ms
FFP2	Free Running Frame Period (R = 408kΩ, C = 220nF)		14.3		ms
FPR	Frame Period Ratio = FFP/MFP	1.7	1.8	1.9	
FG	Frame Saw-tooth Gain Between Pin 1 and non Inverting Input of the Frame Amplifier		-0.4		
$\frac{\Delta F}{\Delta \theta}$	Vertical Frequency Drift with Temperature (see application)		4.10^{-3}		Hz/°C

8215B-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

V_{CC1} = 10V, T_{AMB} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
FRAME POWER SUPPLY (Pin 9)					
V9	Operating Voltage (with flyback Generator)	10		58	V
I9	Supply Current (V9 = 30V)		11	22	mA
FLYBACK GENERATOR SUPPLY (Pin 3)					
$V_{CC}2$	Operating Voltage	10		30	V
FRAME OUTPUT (Pin 10)					
	Saturation Voltage to Ground (V9 = 30V)				
LV10A	I10 = 0.1A		0.06	0.6	V
LV10B	I10 = 1A		0.37	1	V
	Saturation Voltage to V9 (V9 = 30V)				
HV10A	I10 = -0.1A		1.3	1.6	V
HV10B	I10 = -1A		1.7	2.4	V
	Saturation Votage to V9 in Flyback Mode (V10 > V9)				
FV10A	I10 = 0.1A		1.6	2.1	V
FV10B	I10 = 1A		2.5	4.5	V
FLYBACK GENERATOR (Pin 3 and Pin 4)					
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V4/3 with				
F2DA	$I_{4 \rightarrow 3}$ = 0.1A		1.5	2.1	V
F2DB	$I_{4 \rightarrow 3}$ = 1A		3.0	4.5	V
	Flyback Transistor on (output = high state), V_{CC2} = 30V, V3/4 with				
FSVA	$I_{3 \rightarrow 4}$ = 0.1A		0.8	1.1	V
FSVB	$I_{3 \rightarrow 4}$ = 1A		2.2	4.5	V
	Flyback Transistor off (output = V9 - 8V), V9 - V_{CC2} = 30V				
FCI	Leakage Current Pin 3			170	µA
SUPER SANDCASTLE OUTPUT (Pin 19)					
	Output Voltages (R load = 2.2kΩ)				
SANDT2	Frame blanking pulse level	2	2.5	3	V
SANDL2	Line blanking pulse level	4	4.5	5	V
BG2	Burst key pulse level	8	9		V
	Pulses width and timing				
SC3	Delay between middle of sync pulse and leading edge of burst key pulse	2.3	2.7	3.1	µs
SC2	Duration of burst key pulse Vertical blanking pulse width	3.7	4 Note 1	5	µs
LINE FLYBACK INPUT (Pin 18)					
	Switching level		2		V
	Maximum imput current at V_{PEAK} = 800V		8		mA
	Limiting voltage at maximum current		4.3		V
τ	RC network time constant (Note 2)		6		µs

8215B-04.TBL

Notes :
1. Width of vertical blanking pulse on SSC output is proportional to the frame flyback time, the switching level is $V_{CC}2 - 2V_{BE}$ and the other input of the comparator is tied to the frame amplifier output. Application circuit uses the frame flyback generator.
2. An RC network is connected to this input. Typical value for the resistor is 27kΩ and 220pF for the capacitor. A different time constant for RC changes the delay between the middle of the line synchro pulse and the leading edge of the burst key pulse but also the duration of the burst key pulse.

GENERAL DESCRIPTION

The TDA8215B performs all the video and power functions required to provide signals for the line driver and frame yoke.

It contains:
- A synchronization separator
- An integrated frame separator without external components
- A saw-tooth generator for the frame
- A power amplifier for direct drive of frame yoke (short circuit protected)
- An open collector output for the line darlington drive
- A line phase detector and a voltage control oscillator
- A super sandcastle generator
- Video identification output.

The slice level of sync-separation is fixed by value of the external resistors R1 and R2. VR is an internally fixed voltage.

The sync-pulse allows the discharge of the capacitor by a 2 x I current. A line sync-pulse is not able to discharge the capacitor under $V_Z/2$. A frame sync-pulse permits the complete discharge of the capacitor, so during the frame sync-pulse Q_3 and Q_4 provide current for the other parts of the circuit.

Figure 1 : Synchronization Separator Circuit

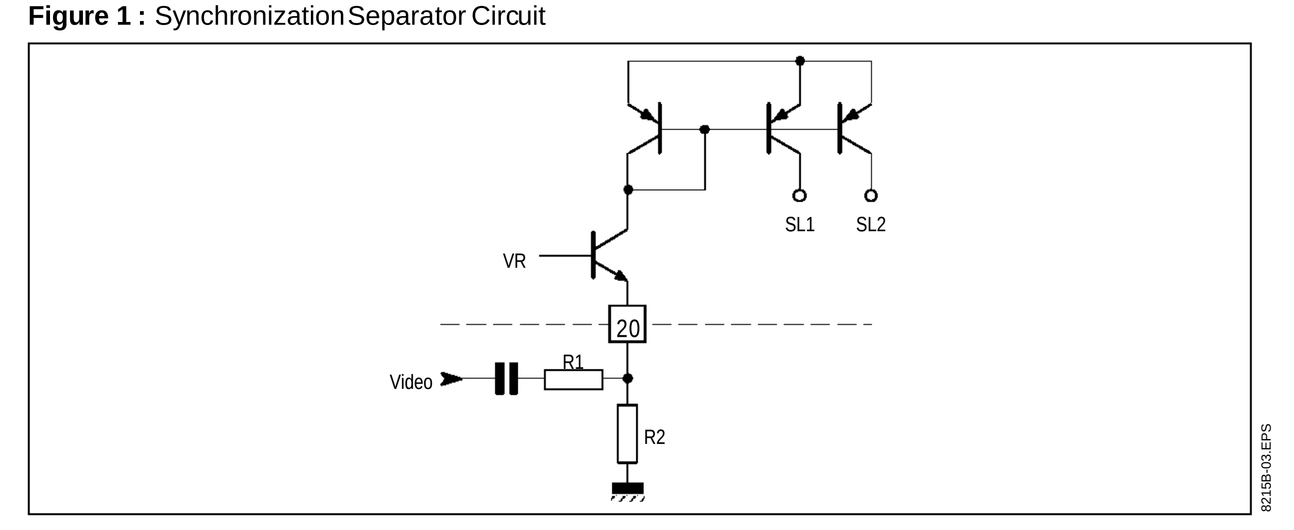


Figure 2 : Frame Separator

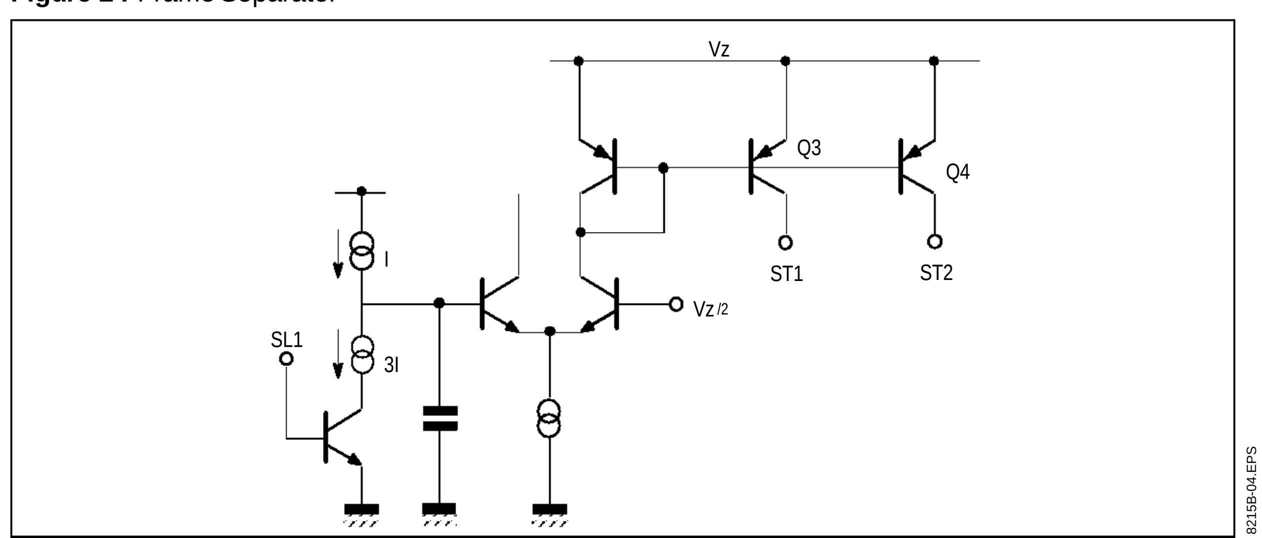
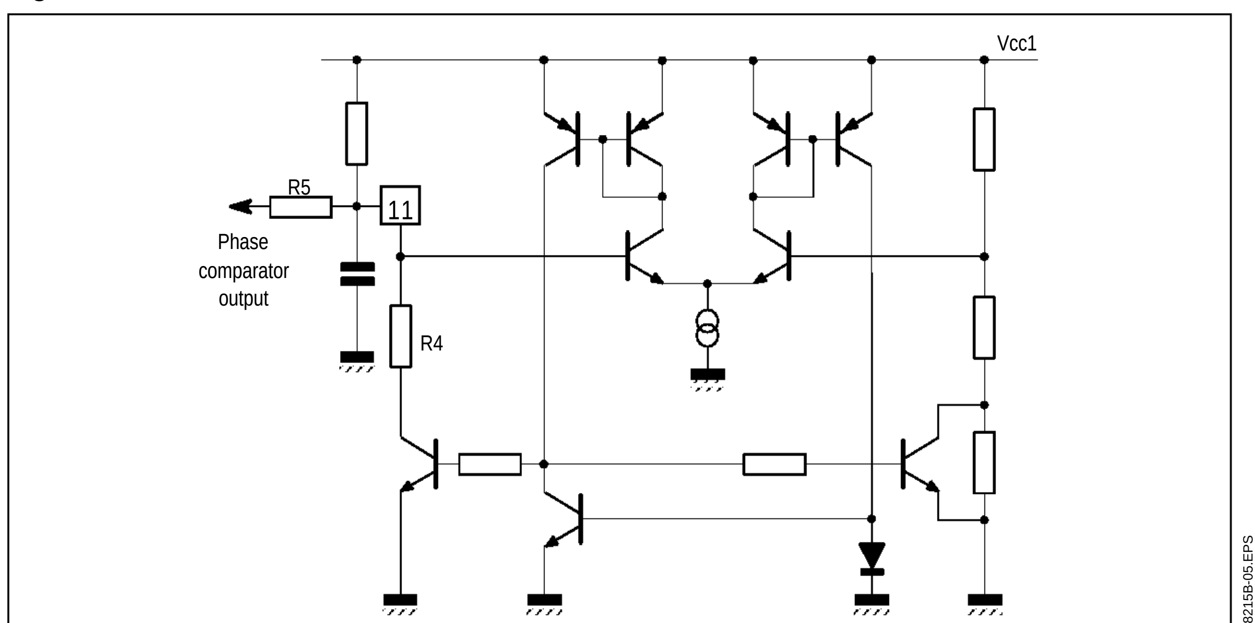
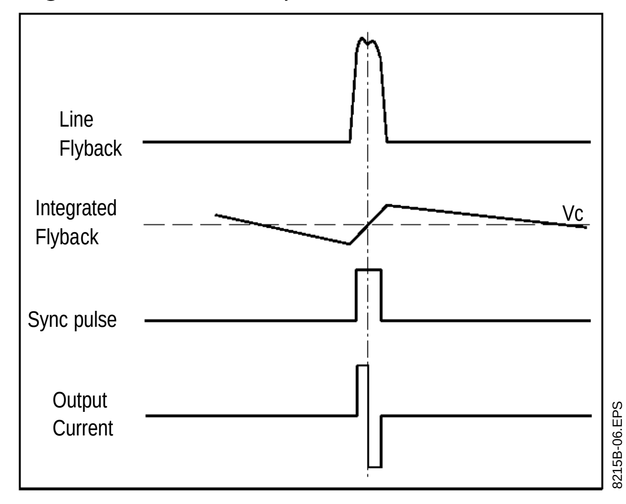


Figure 3 : Line Oscillator



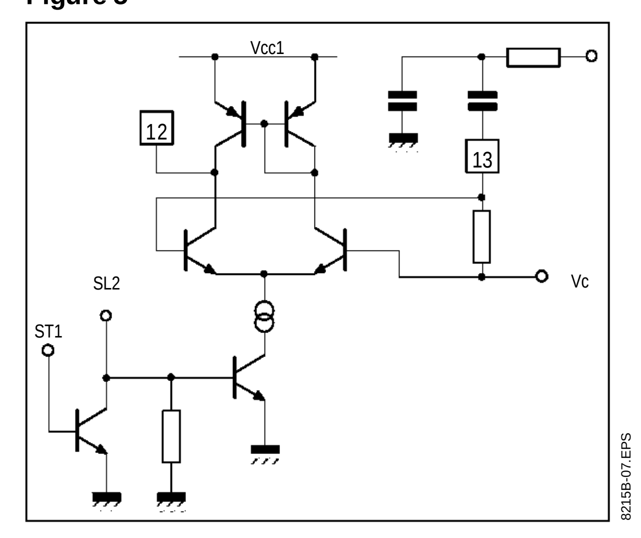
The oscillator thresholds are internally fixed by resistors. The discharge of the capacitor depends on the internal resistor R4. The control voltage is applied on resistor R5.

Figure 4 : Phase Comparator



The sync-pulse drives the current in the comparator. The line flyback integrated by the external net work gives on pin 13 a saw tooth, the DC offset of this saw tooth is fixed by VC. The comparator output provides a positive current for the part of the signal on pin 13 greater than to VC and a negative current for the other part. When the line flyback and the video signal are synchronized, the output of the comparator is an alternatively negative and positive current. The frame sync-pulse inhibits the comparator to prevent frequency drift of the line oscillator on the frame beginning.

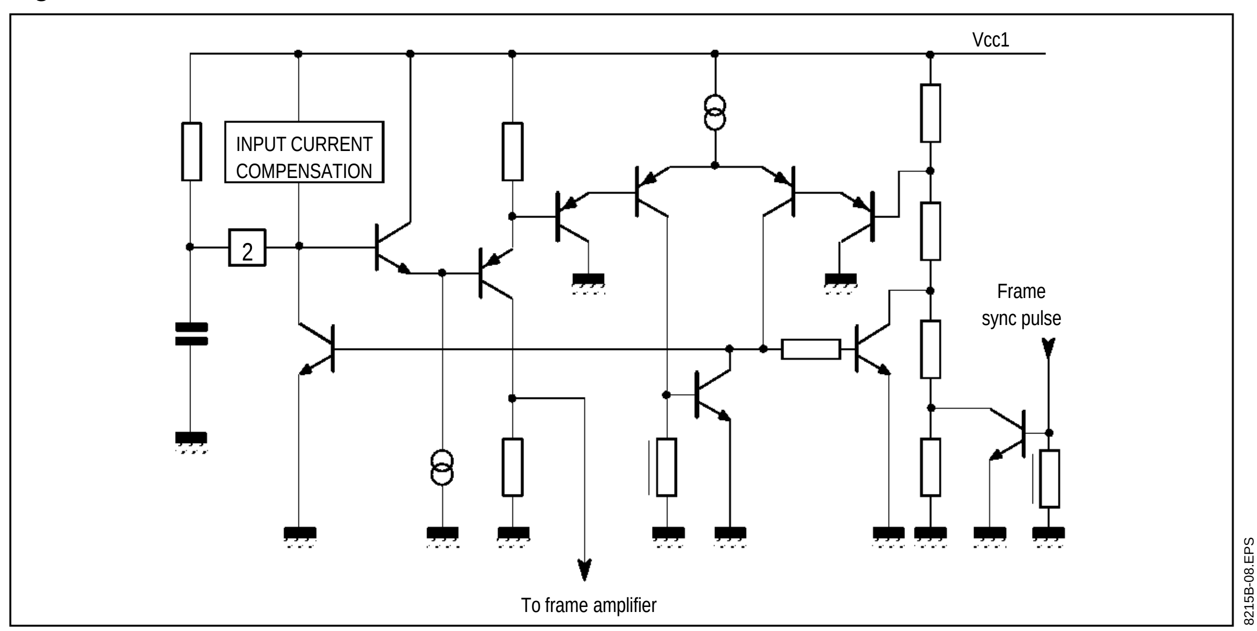
Figure 5



Line output (Pin 17)

It is an open-collector output. The output negative pulse time is 22µs for a 64µs period.
The oscillator thresholds are internally fixed by resistors. The oscillator is synchronized during the last half free run period. The input current during the charge of the capacitor is less than 100nA.

Figure 6 : Frame Oscillator



Frame output amplifier

This amplifier is able to drive directly the frame yoke. Its output is short circuit and overload protected; it contains also a thermal protection.

The frame blanking is detected by the frame flyback generator. When the output voltage of the frame amplifier exceeds $V_{CC}2\text{-}2V_{BE}$, the pulse is detected. The line flyback detection is provided by a comparator which compares the input line flyback pulse to an internal reference. The burst gate pulse position is fixed by the external RC network (Pin 14). It is referenced to the middle of the line flyback.

This stage will detect the coincidence between the line sync pulse (if present) and a 2µs sampling pulse. This 2µs pulse is positionned at the center of line sync pulse when the phase loop is locked. This sampled detection is stored by an external capacitor Pin 8.

The identification output level is high when video signal is present.

Important remark : minimum saw-tooth amplitude on Pin 13 has to be $2V_{PP}$ (typ. : $2.5V_{PP}$).

Figure 7 : Super Sandcastle Generator

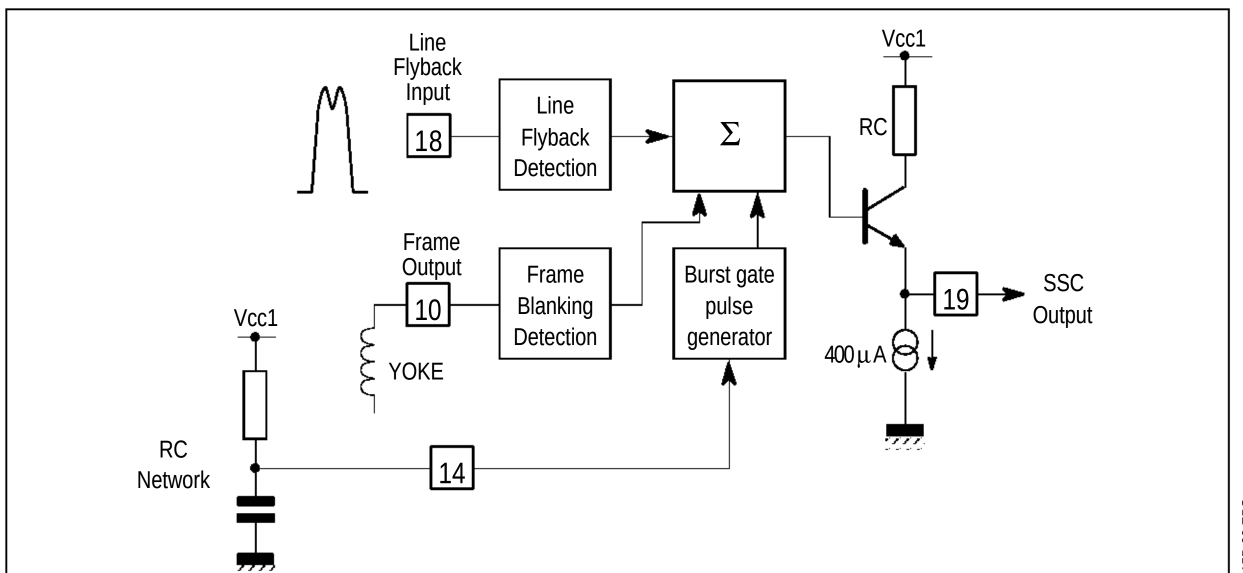
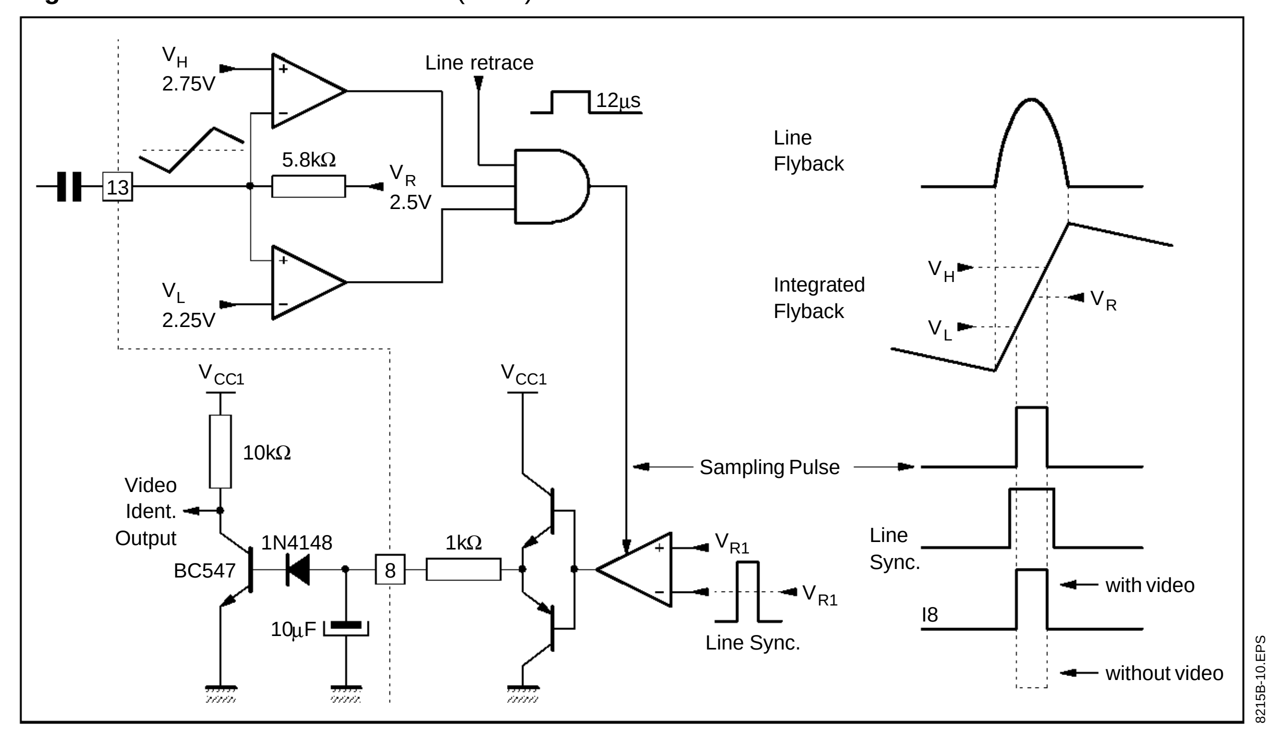
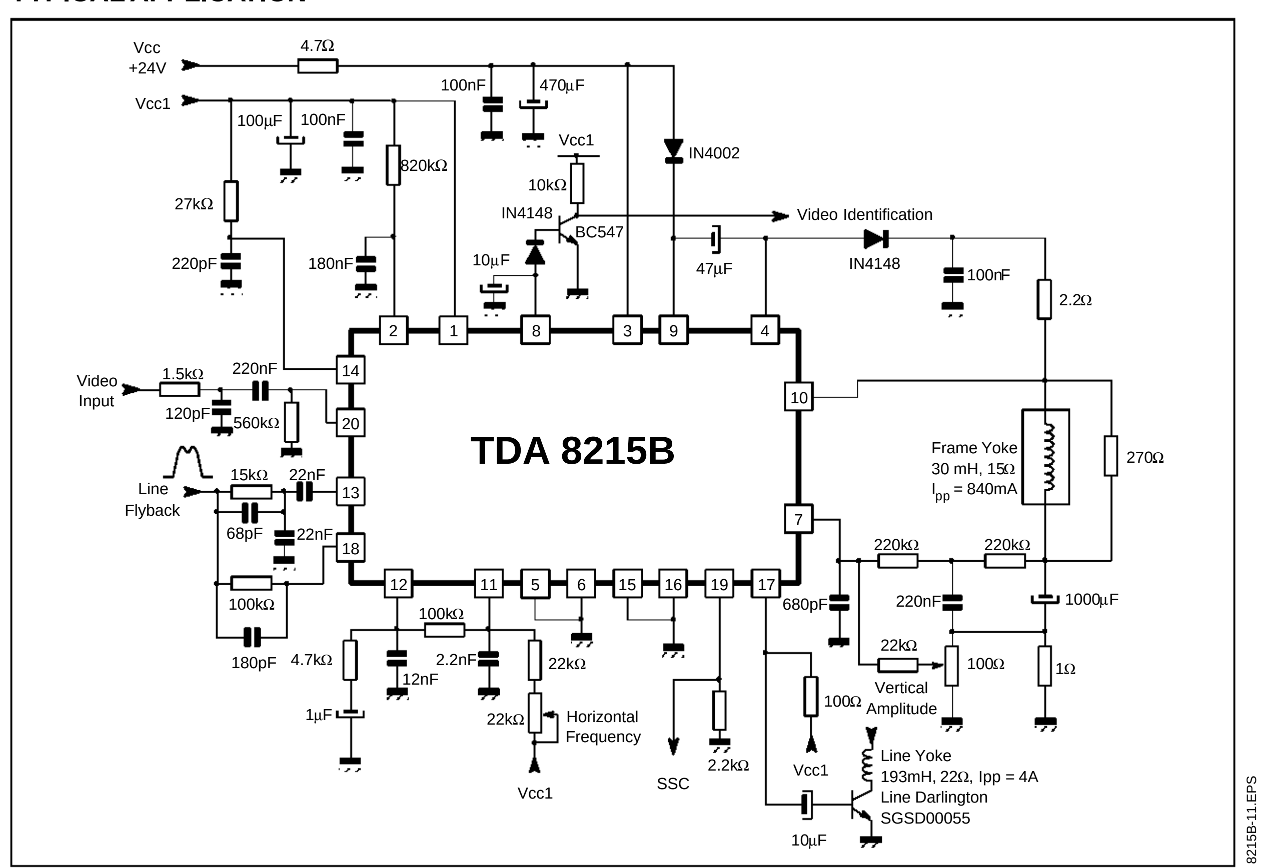


Figure 8 : Video Identification Circuit (Pin 8)

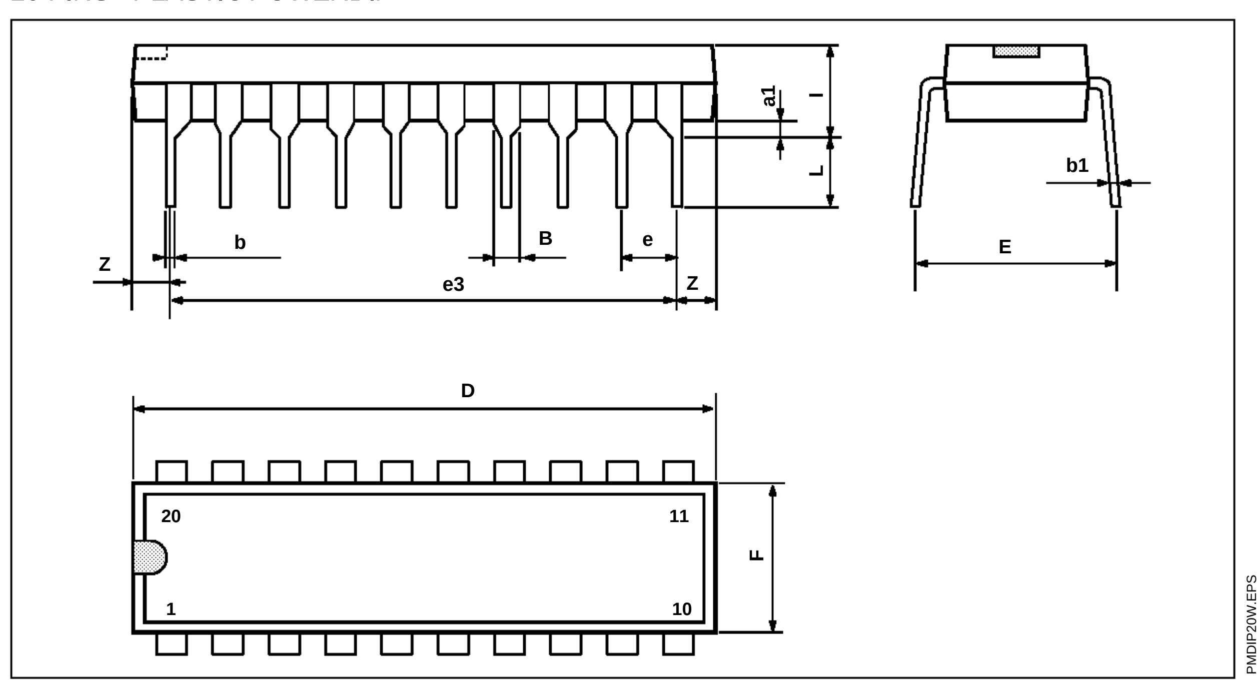


TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

20 PINS - PLASTIC POWERDIP



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

DIP20PW.TBL

